Wire bonding chips to a printed circuit board presents an challenge when representing the entire circuit on the schematic while maintaining a copper netlist in the PCB. In this application note, we present a method that fully represents the connectivity between the die and board in the schematic, while maintaining the copper netlist in the PCB.

**Question:**

Have you ever considered the use of a wire bonded chip on your PCB? Several advantages exist including the ability to reduce the height of the product package; the ability to hide the chip to make reverse engineering difficult; the need to reduce material cost and turn time for high volume production; and the possibility to increase the speed of the overall design by removing a connection point between the PCB, package, and chip.

Altium Designer has the ability to handle the wire bonding using existing capabilities within the tool. This is made possible by using a signal layer in the PCB to represent the die and its connectivity, while making use of the jumper option in the property of the pads primitive. This application note will provide specifics on how to create the library footprint, and how to implement it on the PCB.

Wirebonding is commonly referred to as “chip on board”.

**Procedure:**

Creating a footprint for purposes of wirebonding relies upon meeting 2 objectives. The first objective is to allow the schematic the ability to show the circuit connectivity to the die. Therefore, as part of the libraries, the die will be represented as both a schematic symbol and a PCB footprint.

The connectivity achieved in the schematic is automatically translated to copper connectivity on the PCB. This is desired for packaged components; however, this is not necessary true for wire bonding. Unlike the schematic which may show the connectivity up to and including the die itself, the PCB copper will need to stop at the land pad. The rest of the connectivity to the die has to be accounted for, otherwise Altium will generate numerous DRC errors.

Wire bonding requires the use of 2 features in the PCB library: the jumper option in the pad primitive and the ability to add signal layers.

*The “Wirebonding” Layer*
The first feature is the ability to enable signal mid layers in the PCB library. Normally this practice would be frowned upon since Altium Designer will enable any layer in the PCB that has been implemented in a library component. Though this does not happen too often for signal mid layers, many users stumble upon this issue when they are not careful in assigning mechanical layers.

For wirebonding purposes, a signal mid layer will be dedicated for all primitives that would be associated to the wirebond or the corresponding die. This layer is added to maintain a full netlist synchronization between the schematic and PCB; however, when it comes time for manufacturing files, this mid layer is not generated. Thus, the only the manufacturing files created are the actual copper files.

**The Jumper Makes the Connection**

The jumper option in the pad primitive plays a critical role in making the connection to primitives between the copper layer and the primitives on the wirebonding layer. The jumper allows connectivity between two pads without the need for copper, and allows for connectivity between pads that reside on different layers. In the PCB, the jumper option is not made available. It can only be implemented in the PCB library editor.
In the example illustrations, top layer pad 1 and mid layer (wirebond layer) pad L1 are set with Jumper ID equal to 1. Pad 2 and pad L2 would be set with the Jumper ID equal 2, etc.

It should be noted that 2 different pads names were used for the top and wirebond land pads (in the example, pads "1" and "L1" were used). This is to allow for a schematic representation in which the landing pad will have 2 pins.

**Why 2 Pads For the Landing?**

Without having the 2 pads configured as illustrated, connectivity on the schematic sheet becomes an issue. Though the copper landing pad is physically an end point for the copper on the PCB, it is not an end point for the purposes of connectivity within the schematic. In the schematic, the landing pad actually represents 2 pins, one pin to interface with the other components on the board and the other to interface with the die. Effectively, we have the following representation:
Therefore, rather than jumping the copper land pad directly to the die, we use an intermediary land pad on the wirebonding layer to facilitate the transition from the copper layer to the wirebonding layer.

The Schematic Symbol

One of Altium Designer’s unique library capabilities is to allow a symbol to be created with the intent on adding wires within it after it has been placed on the schematic. This feature allows the user to create a symbol consisting of both land and die pads without the need to dedicate the connectivity between the land and die pads within the footprint or symbolic representations.
In this illustration, the copper land pad, the corresponding land pad on the wirebonding layer, and the die pad are all represented in a single schematic symbol. The user will have the ability to connect the land pads of the wirebonding layer to the die in the schematic editor.

The Schematic Editor

Placement of the symbol into the schematic editor is handled through the usual placement methods. In the example provided, note that the connectivity between the die and the landing pads was demonstrated using various wiring styles. All of these styles can be achieved by pressing SHIFT - Spacebar when placing the wire. In this particular example, 4 headers were added to show connectivity outside of the landing pads.
This illustration shows the symbol connected to four headers. Note the various methods of connecting the die pins to the wirebonding pins. All of these methods of drawing the wire connectivity can be achieved through SHIFT-SpaceBar.

PCB Editor

Pushing the information from the schematic to PCB is performed using the standard ECO process. When completed, Altium Designer will automatically add the signal midlayer (since it was defined in the library):
Place the copper as you would normally do so. As for the connection on the wirebonding layer, you should place wires from the landing pads to the die to avoid DRC errors.

The illustration on the left shows the completed routing of the PCB board. The second illustration shows the connectivity of the land pads to the pad.
The project created to demonstrate these concepts is available upon request. Please contact your Altium representative or use your Support Center login to create a case support case.